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Holden et al.

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(45) **Date of Patent: Oct. 4, 2016**

(54) **ORTHOGONAL DIFFERENTIAL VECTOR SIGNALING CODES WITH EMBEDDED CLOCK**

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(21) Appl. No.: **14/816,896**

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(51) **Int. Cl.**
H04L 27/04 (2006.01)
H04L 27/26 (2006.01)

(52) **U.S. Cl.**
CPC ***H04L 27/2637*** (2013.01)

(58) **Field of Classification Search**
CPC H04L 27/04; H03M 3/00
See application file for complete search history.

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(Continued)

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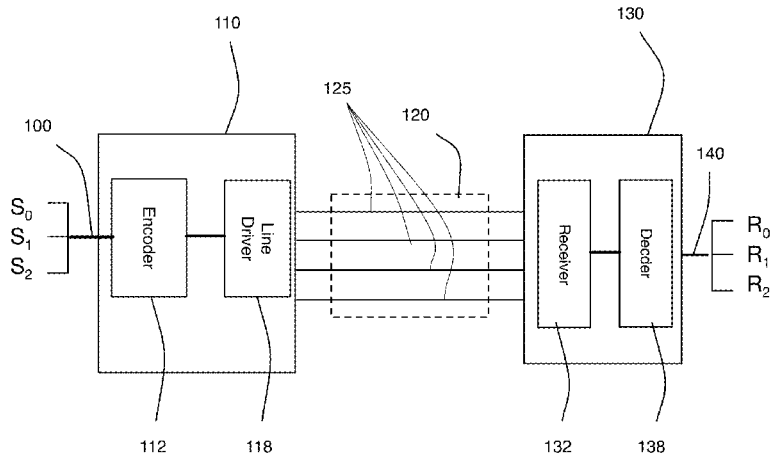
(74) *Attorney, Agent, or Firm* — Invention Mine LLC

(57) **ABSTRACT**

Orthogonal differential vector signaling codes are described which support encoded sub-channels allowing transport of distinct but temporally aligned data and clocking signals over the same transport medium. Embodiments providing enhanced LPDDR interfaces are described which are suitable for implementation in both conventional high-speed CMOS and DRAM integrated circuit processes.

19 Claims, 10 Drawing Sheets



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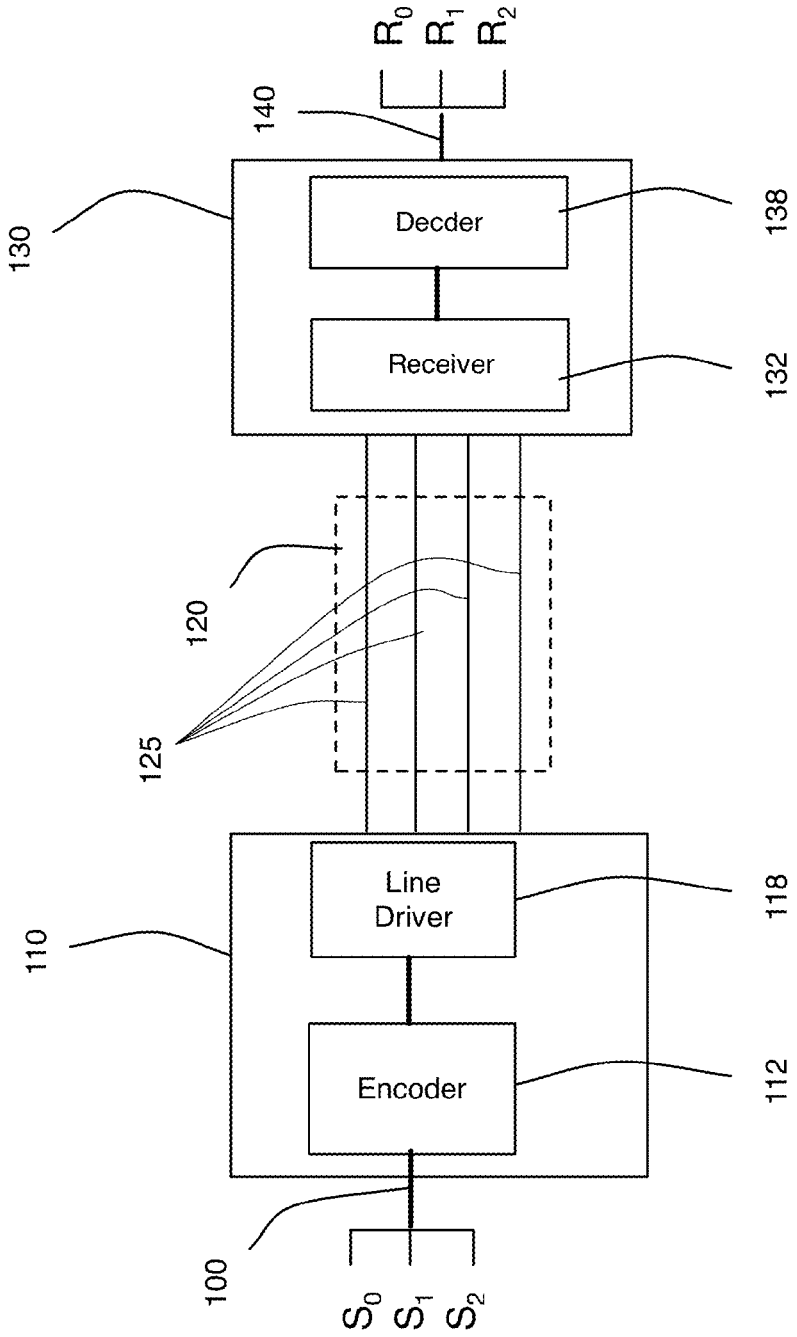
R_0 R_1 R_2
140
130
Decder
138
Receiver
132
120
125
Line Driver
118
110
Encoder
112
100
S_0 S_1 S_2

FIG. 1

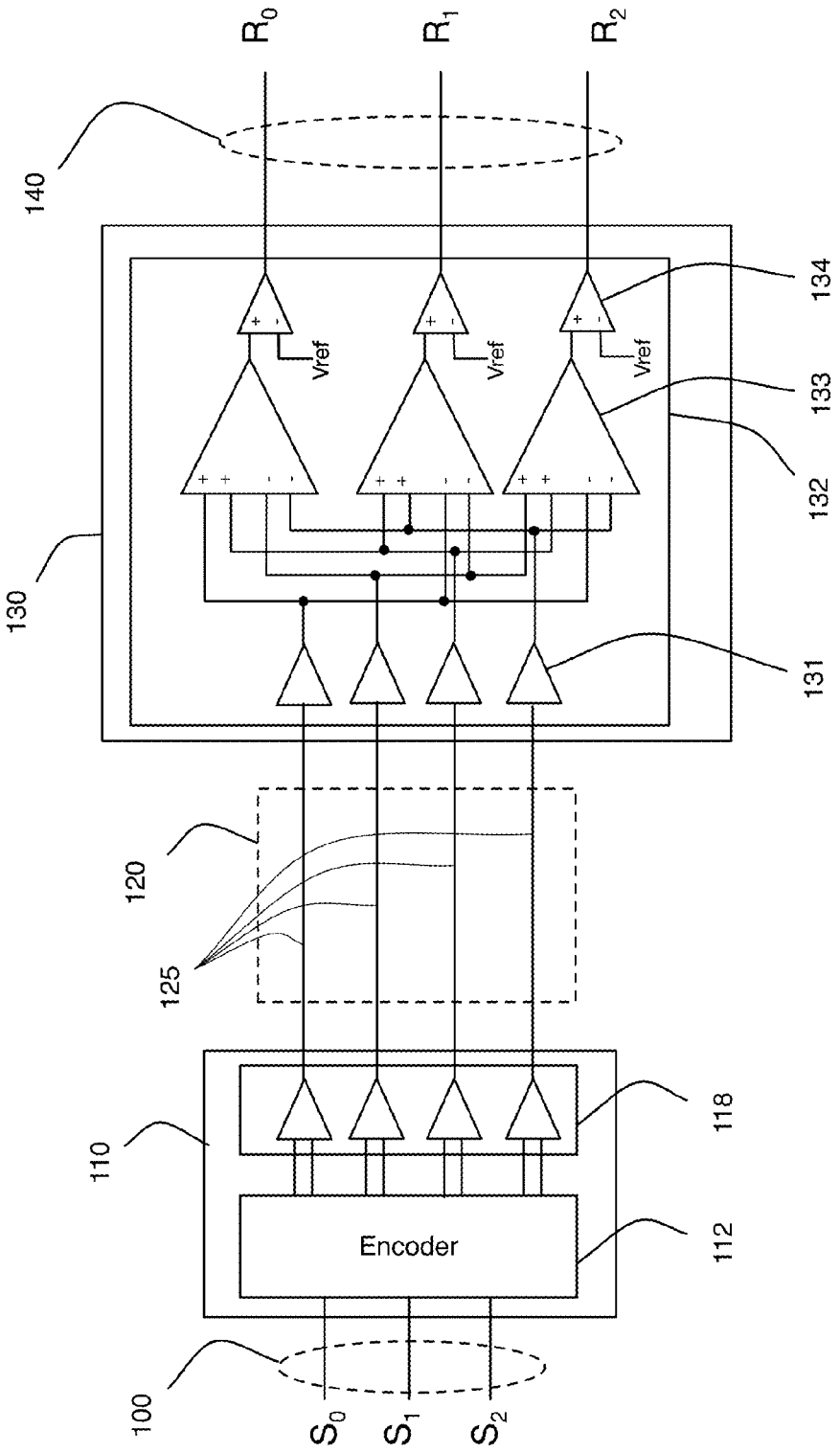
R0
R1
R2
140
134
133
132
130
131
Vref
Vref
Vref
120
125
110
118
Encoder
112
100
S0
S1
S2

FIG. 2

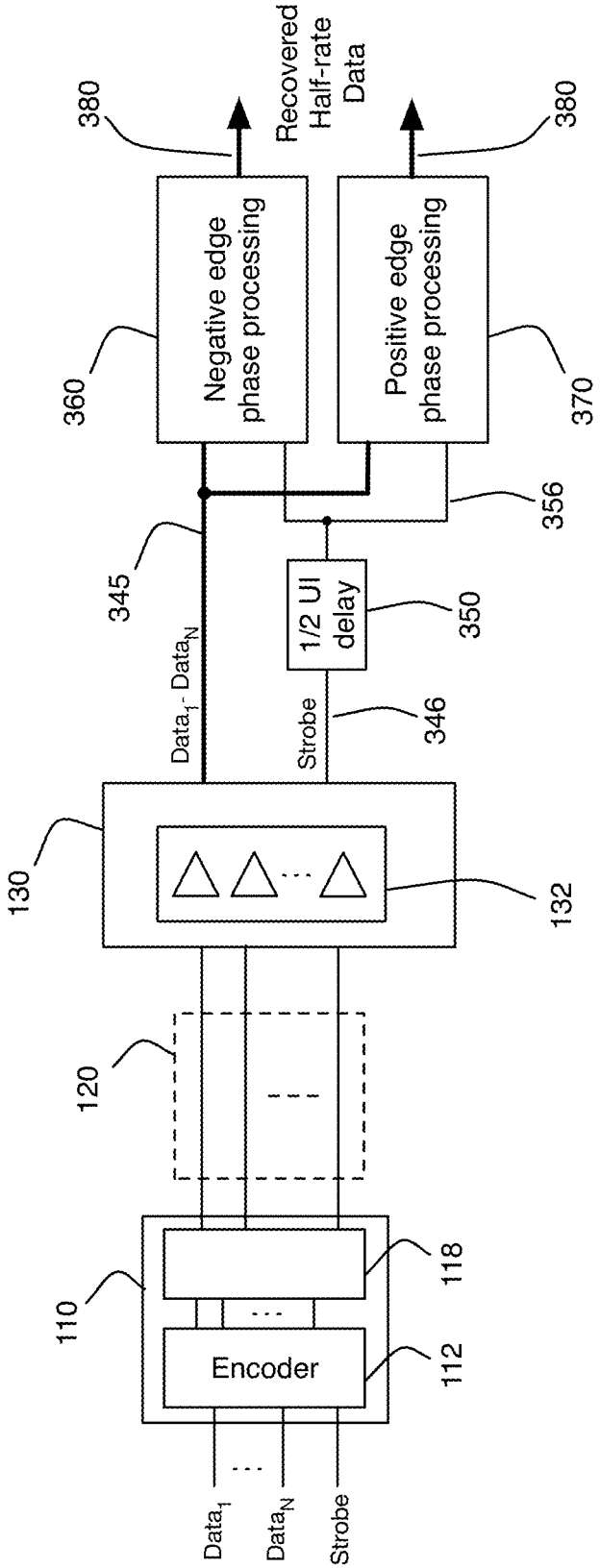
Recovered Half-rate Data
380
380
Negative edge phase processing
Positive edge phase processing
360
370
356
345
1/2 UI delay
350
Data1- DataN
Strobe
346
130
132
120
110
118
Encoder
112
Data1
DataN
Strobe

FIG. 3

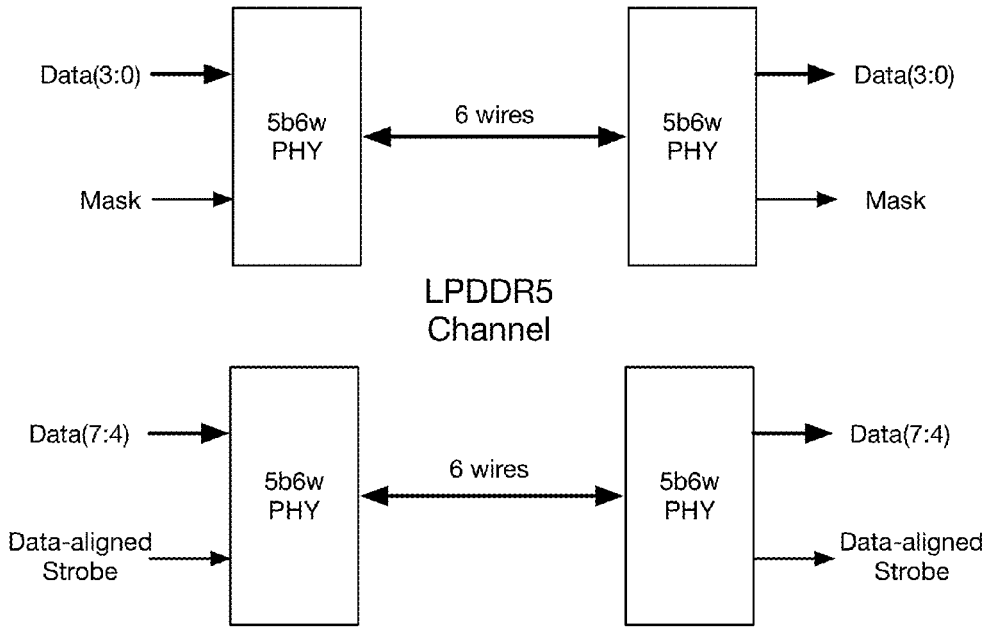
Data(3:0)
Mask
5b6w PHY
6 wires
5b6w PHY
Data(3:0)
Mask
LPDDR5 Channel
Data(7:4)
Data-aligned Strobe
5b6w PHY
6 wires
5b6w PHY
Data(7:4)
Data-aligned Strobe

FIG. 4

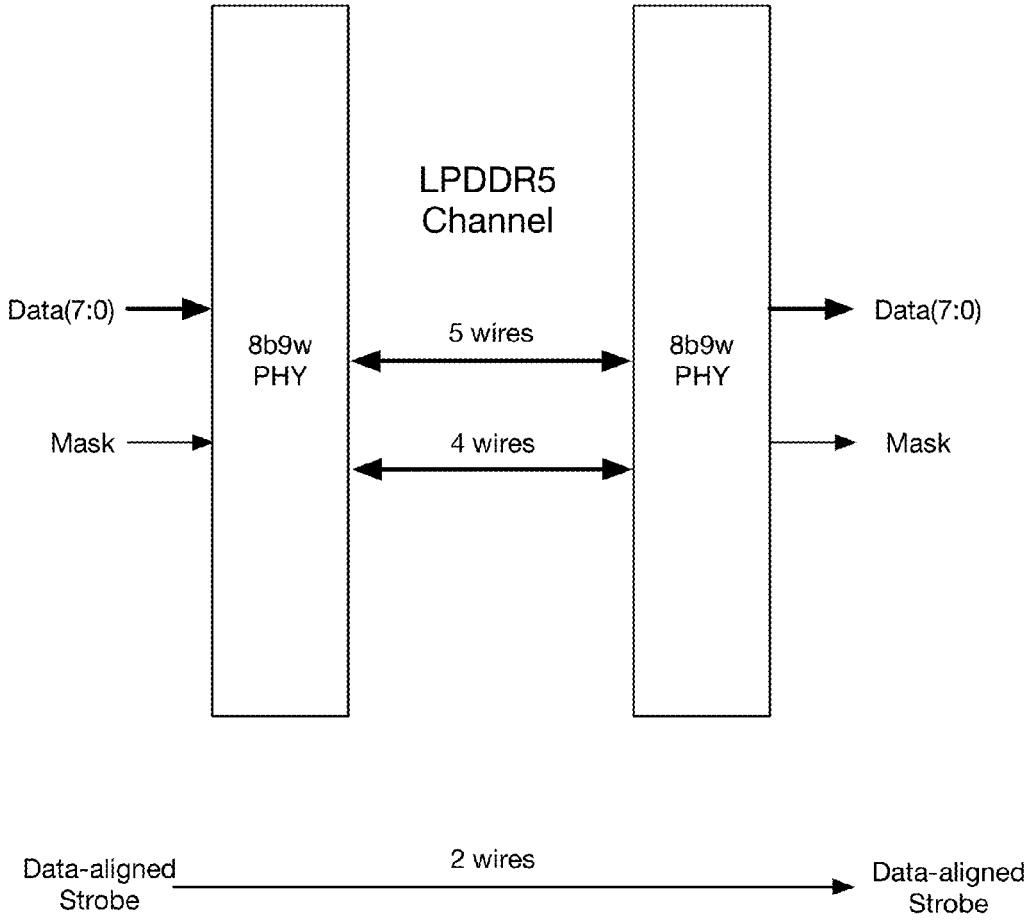
LPDDR5
Channel
Data(7:0)
Mask
8b9w
PHY
5 wires
4 wires
8b9w
PHY
Data(7:0)
Mask
Data-aligned
Strobe
2 wires
Data-aligned
Strobe

FIG. 5

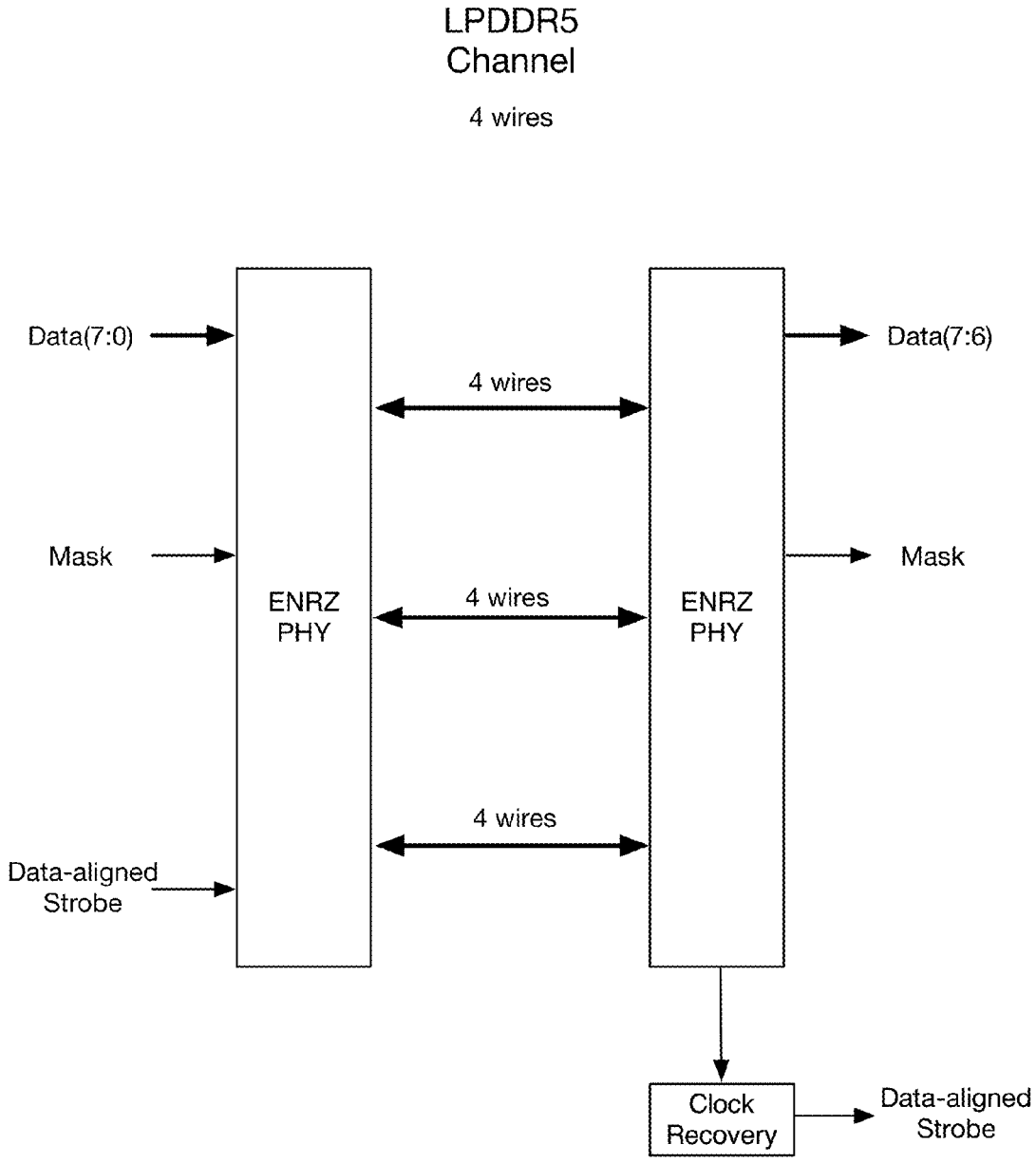
LPDDR5
Channel
4 wires
Data(7:0)
Mask
Data-aligned
Strobe
ENRZ
PHY
4 wires
4 wires
4 wires
ENRZ
PHY
Data(7:6)
Mask
Clock
Recovery
Data-aligned
Strobe

FIG. 6

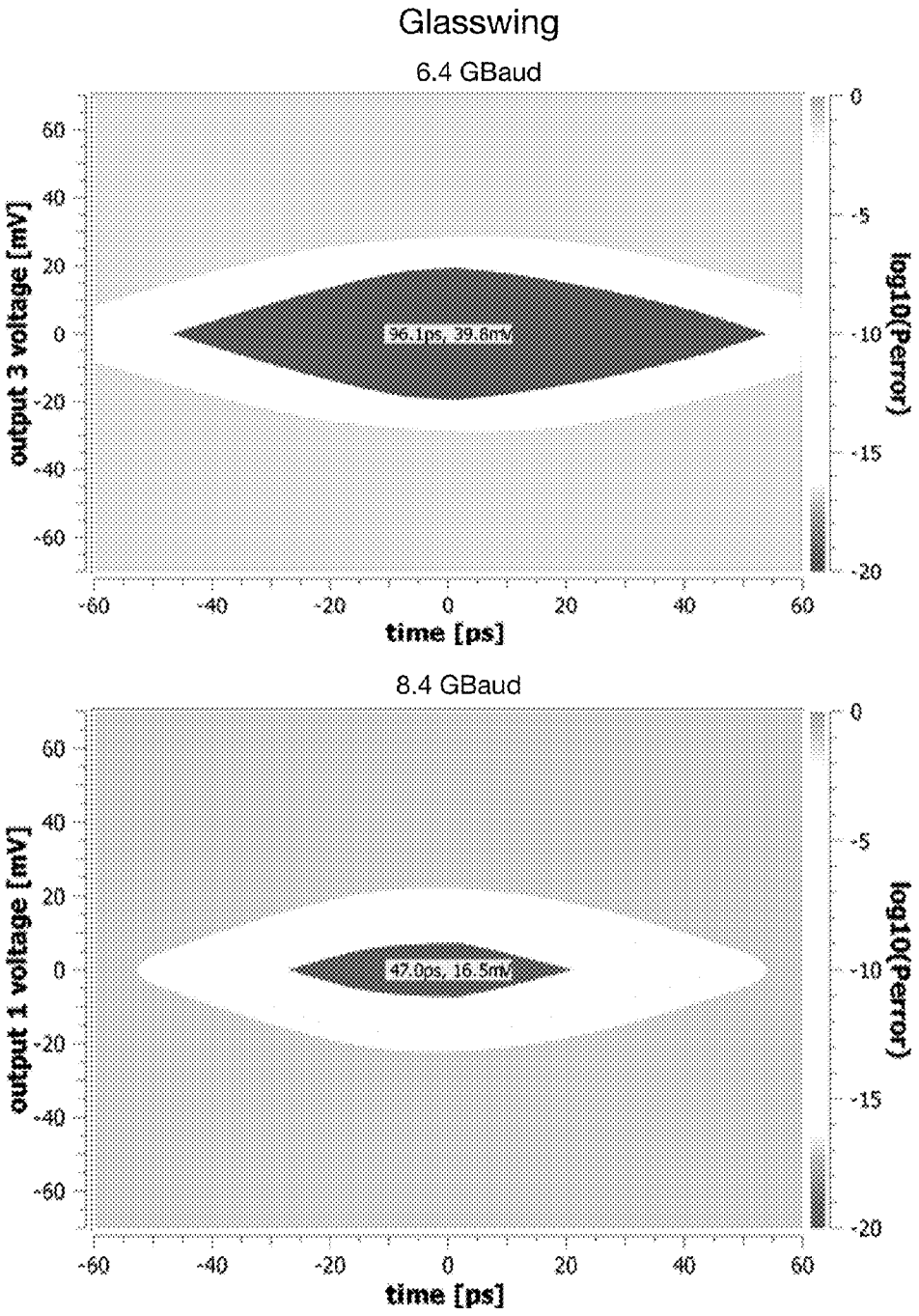
Glasswing
6.4 GBaud
output 3 voltage [mV]
time [ps]
log10(Perror)
96.1ps, 39.6mV
8.4 GBaud
output 1 voltage [mV]
time [ps]
log10(Perror)
47.0ps, 16.5mV

FIG. 7A

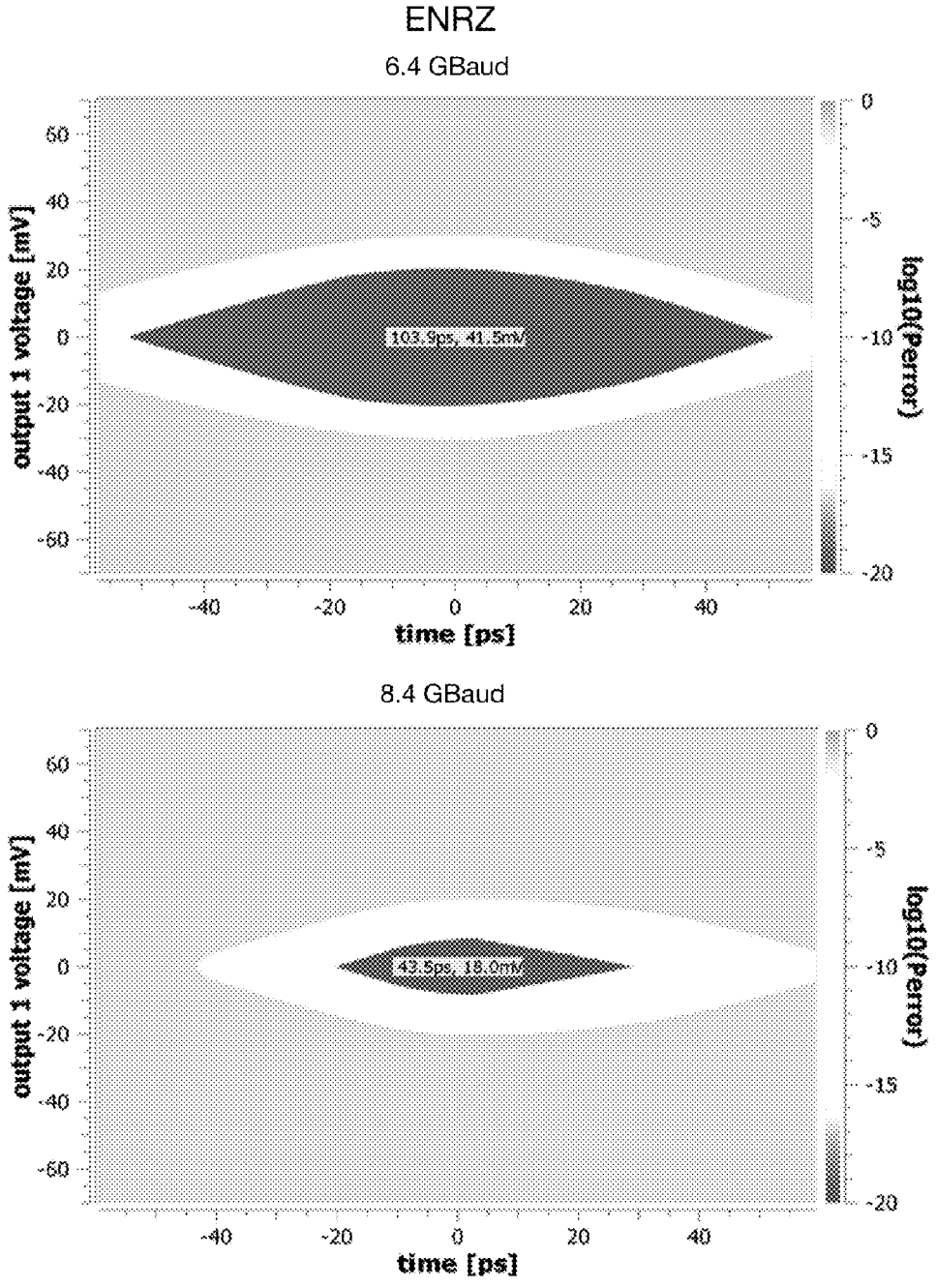
ENRZ
6.4 GBaud
103.9ps, 41.5mV
output 1 voltage [mV]
time [ps]
log10(Perror)
8.4 GBaud
43.5ps, 18.0mV
output 1 voltage [mV]
time [ps]
log10(Perror)

FIG. 7B

8b9w

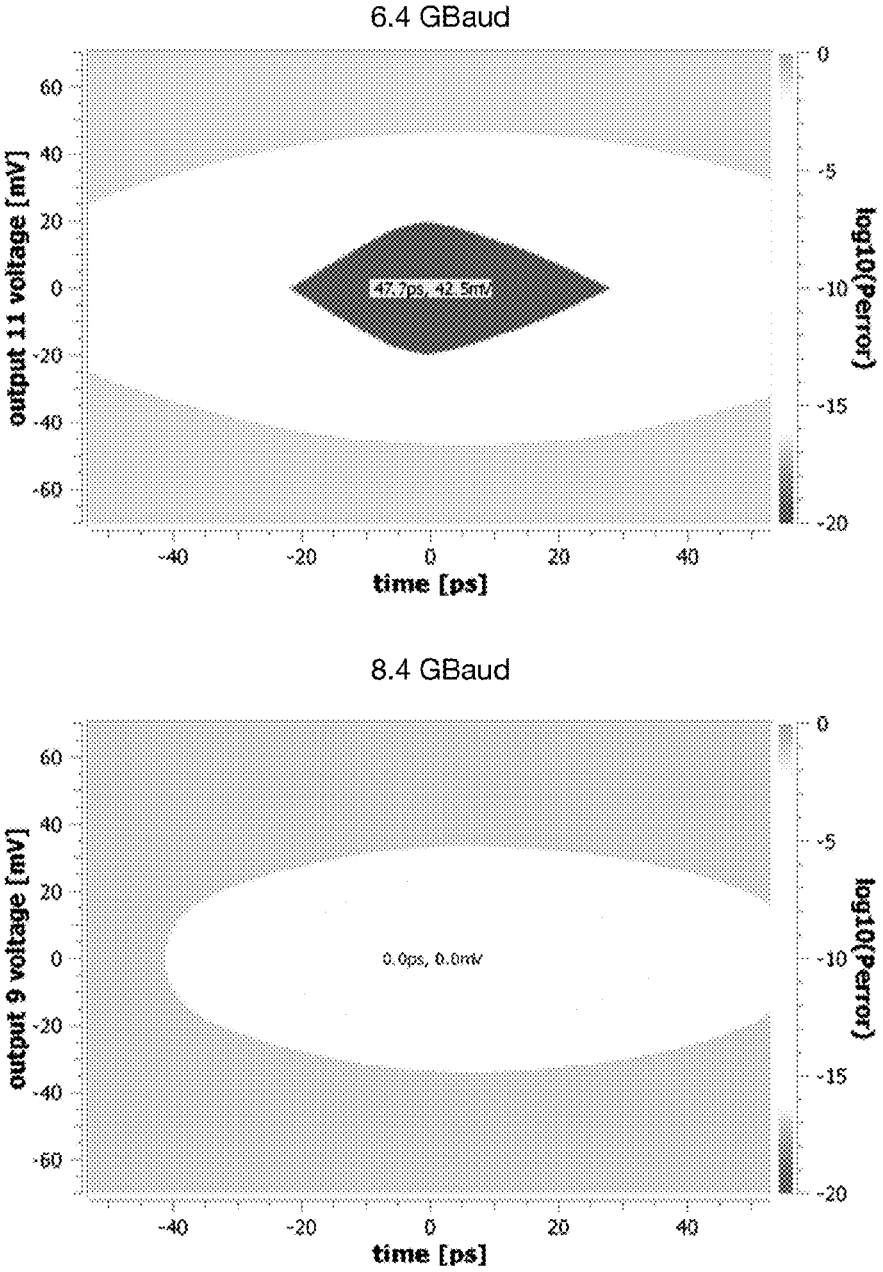
6.4 GBaud
output 11 voltage [mV]
time [ps]
log10(Perror)
47.7ps, 42.5mV
8.4 GBaud
output 9 voltage [mV]
time [ps]
log10(Perror)
0.0ps, 0.0mV

FIG. 7C

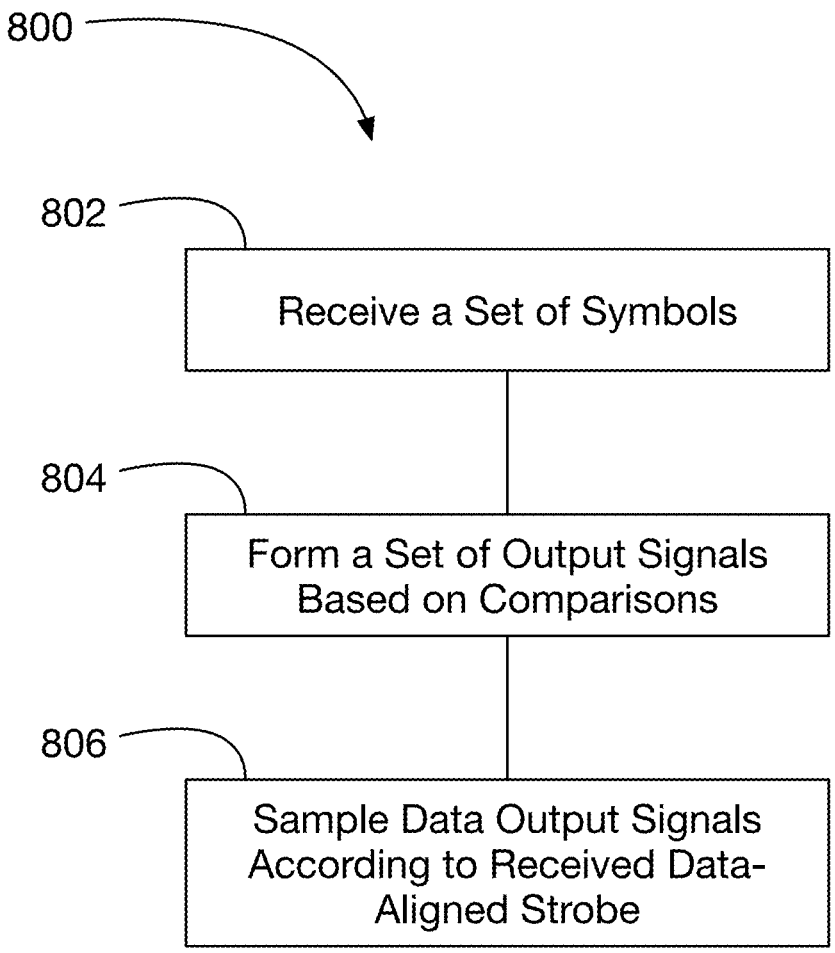
800
802
Receive a Set of Symbols
804
Form a Set of Output Signals Based on Comparisons
806
Sample Data Output Signals According to Received Data-Aligned Strobe

FIG. 8

ORTHOGONAL DIFFERENTIAL VECTOR SIGNALING CODES WITH EMBEDDED CLOCK

This application claims priority to U.S. Provisional Patent Application 62/032,175, filed Aug. 1, 2014, naming Brian Holden and Amin Shokrollahi, entitled "Orthogonal Differential Vector Signaling Codes with Embedded Clock," which is hereby incorporated herein by reference in its entirety for all purposes.

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The following references are herein incorporated by reference in their entirety for all purposes:

U.S. Patent Publication No. 2011/0268225 of U.S. patent application Ser. No. 12/784,414, filed May 20, 2010, naming Harm Cronie and Amin Shokrollahi, entitled "Orthogonal Differential Vector Signaling", hereinafter identified as [Cronie I];

U.S. patent application Ser. No. 13/030,027, filed Feb. 17, 2011, naming Harm Cronie, Amin Shokrollahi and Armin Tajalli, entitled "Methods and Systems for Noise Resilient, Pin-Efficient and Low Power Communications with Sparse Signaling Codes", hereinafter identified as [Cronie II];

U.S. patent application Ser. No. 14/158,452, filed Jan. 17, 2014, naming John Fox, Brian Holden, Peter Hunt, John D Keay, Amin Shokrollahi, Richard Simpson, Anant Singh, Andrew Kevin John Stewart, and Giuseppe Surace, entitled "Chip-to-Chip Communication with Reduced SSO Noise", hereinafter identified as [Fox I];

U.S. patent application Ser. No. 13/842,740, filed Mar. 15, 2013, naming Brian Holden, Amin Shokrollahi and Anant Singh, entitled "Methods and Systems for Skew Tolerance in and Advanced Detectors for Vector Signaling Codes for Chip-to-Chip Communication", hereinafter identified as [Holden I];

U.S. Provisional Patent Application No. 61/934,804, filed Feb. 2, 2014, naming Ali Hormati and Amin Shokrollahi, entitled "Methods for Code Evaluation Using ISI Ratio", hereinafter identified as [Hormati I];

U.S. Provisional Patent Application No. 61/934,807, filed Feb. 2, 2014, naming Amin Shokrollahi, entitled "Vector Signaling Codes with High pin-efficiency and their Application to Chip-to-Chip Communications and Storage", hereinafter identified as [Shokrollahi I];

U.S. Provisional Patent Application No. 61/839,360, filed Jun. 23, 2013, naming Amin Shokrollahi, entitled "Vector Signaling Codes with Reduced Receiver Complexity", hereinafter identified as [Shokrollahi II].

U.S. Provisional Patent Application No. 61/946,574, filed Feb. 28, 2014, naming Amin Shokrollahi, Brian Holden, and Richard Simpson, entitled "Clock Embedded Vector Signaling Codes", hereinafter identified as [Shokrollahi III].

U.S. Provisional Patent Application No. 62/015,172, filed Jul. 10, 2014, naming Amin Shokrollahi and Roger Ulrich, entitled "Vector Signaling Codes with Increased Signal to Noise Characteristics", hereinafter identified as [Shokrollahi IV].

U.S. patent application Ser. No. 13/895,206, filed May 15, 2013, naming Roger Ulrich and Peter Hunt, entitled "Circuits for Efficient Detection of Vector Signaling Codes for Chip-to-Chip Communications using Sums of Differences", hereinafter identified as [Ulrich I].

U.S. Provisional Patent Application No. 62/026,860, filed Jul. 21, 2014, naming Roger Ulrich and Amin Shokrollahi, entitled "Bus Reversible Orthogonal Differential Vector Signaling Codes", hereinafter identified as [Ulrich II].

The following additional references to prior art have been cited in this application:

U.S. Pat. No. 7,053,802, filed Apr. 22, 2004 and issued May 30, 2006, naming William Cornelius, entitled "Single-Ended Balance-Coded Interface with Embedded-Timing", hereinafter identified as [Cornelius];

U.S. Pat. No. 8,064,535, filed Mar. 2, 2007 and issued Nov. 22, 2011, naming George Wiley, entitled "Three Phase and Polarity Encoded Serial Interface, hereinafter identified as [Wiley].

U.S. Pat. No. 8,649,460, filed Mar. 11, 2010 and issued Feb. 11, 2014, naming Frederick Ware and Jade Kizer, entitled "Techniques for Multi-Wire Encoding with an Embedded Clock", hereinafter identified as [Ware].

BACKGROUND

In communication systems, a goal is to transport information from one physical location to another. It is typically desirable that the transport of this information is reliable, is fast and consumes a minimal amount of resources. One common information transfer medium is the serial communications link, which may be based on a single wire circuit relative to ground or other common reference, or multiple such circuits relative to ground or other common reference. A common example uses singled-ended signaling ("SES"). SES operates by sending a signal on one wire, and measuring the signal relative to a fixed reference at the receiver. A serial communication link may also be based on multiple circuits used in relation to each other. A common example of the latter uses differential signaling ("DS"). Differential signaling operates by sending a signal on one wire and the opposite of that signal on a matching wire. The signal information is represented by the difference between the wires, rather than their absolute values relative to ground or other fixed reference.

There are a number of signaling methods that maintain the desirable properties of DS while increasing pin efficiency over DS. Vector signaling is a method of signaling. With vector signaling, a plurality of signals on a plurality of wires is considered collectively although each of the plurality of signals might be independent. Each of the collective signals is referred to as a component and the number of plurality of wires is referred to as the "dimension" of the vector. In some embodiments, the signal on one wire is entirely dependent on the signal on another wire, as is the case with DS pairs, so in some cases the dimension of the vector might refer to the number of degrees of freedom of signals on the plurality of wires instead of exactly the number of wires in the plurality of wires.

Any suitable subset of a vector signaling code denotes a "sub code" of that code. Such a subcode may itself be a vector signaling code. With binary vector signaling, each component or "symbol" of the vector takes on one of two possible values. With non-binary vector signaling, each symbol has a value that is a selection from a set of more than two possible values. When transmitted as physical signals on a communications medium, symbols may be represented by particular physical values appropriate to that medium; as examples, in one embodiment a voltage of 150 mV may represent a "+1" symbol and a voltage of 50 mV may represent a "−1" symbol, while in another embodiment "+1" may be represented by 800 mV and "−1" as −800 mV.

A vector signaling code, as described herein, is a collection C of vectors of the same length N, called codewords.

The ratio between the binary logarithm of the size of C and the length N is called the pin-efficiency of the vector signaling code. The Orthogonal Differential Vector Signaling codes of [Cronie I], [Cronie II], [Fox I], [Shokrollahi I], [Shokrollahi II], and [Shokrollahi III] are examples of vector signaling codes, and are used herein for descriptive purposes.

FIG. **1** illustrates a communication system employing vector signaling codes. Bits S**0**, S**1**, S**2** enter block-wise **100** into an encoder **105**. The size of the block may vary and depends on the parameters of the vector signaling code. The encoder generates a codeword of the vector signaling code for which the system is designed. In operation, the encoder may generate information used to control PMOS and NMOS transistors within driver **110**, generating voltages or currents on the N communication wires **125** comprising the communications channel **120**. Receiver **132** reads the signals on the wires, possibly including amplification, frequency compensation, and common mode signal cancellation. Receiver **132** provides its results to decoder **138**, which recreates the input bits at **140**, here shown as received bits R**0**, R**1**, R**2**.

Depending on which vector signaling code is used, there may be no decoder, or no encoder, or neither a decoder nor an encoder. For example, for the 8b8w code disclosed in [Cronie II], both encoder **112** and decoder **1138** exist. On the other hand, for the Hadamard code disclosed in [Cronie I], an explicit decoder may be unnecessary, as the system may be configured such that receiver **132** generates output bits **140** directly.

The operation of the transmitting device **110**, comprising input data **100** and elements **112** and **118**, and that of the receiving device **130**, including element **132**, optional element **138**, and output data **140**, have to be completely synchronized in order to guarantee correct functioning of the communication system. In some embodiments, this synchronization is performed by an external clock shared between the transmitter and the receiver. Other embodiments may combine the clock function with one or more of the data channels, as in the well-known Biphase encoding used for serial communications.

One important example is provided by memory interfaces in which a clock is generated on the controller and shared with the memory device. The memory device may use the clock information for its internal memory operations, as well as for I/O. Because of the burstiness and the asynchronicity of memory operations, the I/O may not be active all the time. Moreover, the main clock and the data lines may not be aligned due to skew. In such cases, additional strobe signals are used to indicate when to read and write the data.

BRIEF DESCRIPTION

Orthogonal differential vector signaling codes providing transport for both data and a clocking signal are described which are suitable for implementation in both conventional high-speed CMOS and DRAM integrated circuit processes. Example channels derived from current practice for Low-Powered DDR4 interfaces are described, as are modest channel enhancements providing higher speed and greater signal integrity.

BRIEF DESCRIPTION OF FIGURES

FIG. **1** illustrates a communication system employing vector signaling codes.

FIG. **2** illustrates one embodiment of an ODVS communications system in which a discrete decoding function is not required.

FIG. **3** is a block diagram of an embodiment transporting data and a clock signal using ODVS code, and incorporating elements facilitating integration of the receiver with conventional DRAM practice.

FIG. **4** is a block diagram of an embodiment utilizing 5b6w code, also known as Glasswing, to implement transport over a proposed LPDDR5 channel.

FIG. **5** is a block diagram of an embodiment utilizing 8b9w code to implement transport over a proposed LPDDR5 channel.

FIG. **6** is a block diagram of an embodiment utilizing ENRZ code to implement transport over a proposed LPDDR5 channel.

FIGS. **7**A, **7**B, and **7**C shows comparative receive eye diagrams for Glasswing, ENRZ, and 8b9w embodiments, respectively, operating at 6.4 GBaud and 8.4 GBaud signaling rates.

FIG. **8** depicts a process in accordance with at least one embodiment.

DETAILED DESCRIPTION

FIG. **1** illustrates a communication system employing vector signaling codes. Source data to transmitter **110**, herein illustrated as S**0**, S**1**, S**2** enter block-wise **100** into encoder **112**. The size of the block may vary and depends on the parameters of the vector signaling code. The encoder **112** generates a codeword of the vector signaling code for which the system is designed. In operation, the codeword produced by encoder **112** is used to control PMOS and NMOS transistors within driver **118**, generating two, three, or more distinct voltages or currents on each of the N communication wires **125** of communications channel **120**, to represent the N symbols of the codeword. Within communications receiver **130**, receiver **132** reads the voltages or currents on the N wires **125**, possibly including amplification, frequency compensation, and common mode signal cancellation, providing its results to decoder **138**, which recreates the input bits as received results **140**, herein shown as R**0**, R**1**, R**2**. As will be readily apparent, different codes may be associated with different block sizes and different codeword sizes; for descriptive convenience and without implying limitation, the example of FIG. **1** illustrates a system using an ODVS code capable of encoding a three binary bit value for transmission over four wires, a so-called 3b4w code.

Depending on which vector signaling code is used, there may be no decoder, or no encoder, or neither a decoder nor an encoder. For example, for the 8b8w code disclosed in [Cronie II], both encoder **112** and decoder **138** exist. On the other hand, for the H4 code disclosed in [Cronie I] (also described herein as ENRZ,) an explicit decoder may be unnecessary, as the system may be configured such that receiver **132** generates the received results **140** directly.

The operation of the communications transmitter **110** and communications receiver **130** have to be completely synchronized in order to guarantee correct functioning of the communication system. In some embodiments, this synchronization is performed by an external clock shared between the transmitter and the receiver. Other embodiments may combine the clock function with one or more of the data channels, as in the well-known Biphase encoding used for serial communications.

One important example is provided by memory interfaces in which a clock is generated on the controller and shared

with the memory device. The memory device may use the clock information for its internal memory operations, as well as for I/O. Because of the burstiness and the asynchronicity of memory operations, the I/O may not be active all the time. Moreover, the main clock and the data lines may not be aligned due to skew. In such cases, additional strobe signals are used to indicate when to read and write the data.

The interface between a system memory controller and multiple Dynamic RAM devices has been well optimized over multiple design generations for both transfer speed and low power consumption. The present state of the art DRAM interface, LPDDR4, includes 8 data lines, 1 DMI signal, 2 strobe lines, as well as other non-data-transfer related lines.

There is considerable interest in extending LPDDR4 to support higher performance at equal or less power consumption, but simple performance extrapolations of the existing technology seem problematic. Decreasing signal integrity precludes simply raising data transfer rates using the existing single-ended interconnection, and misalignment of received DRAM data and its strobe signal is a known issue even at current clock speeds. However, introduction of new technology is constrained by a strong desire to retain as much of the conventional practice as possible regarding bus layout, signal distribution, clocking, etc., as well as a hard requirement that the new technology be implementable in both the high-speed CMOS process used for memory controllers, and in the highly specialized DRAM fabrication process which produces extremely small, high capacitance and low leakage memory cells, but comparatively slow digital and interface logic.

Because of this slow logic speed, conventional DRAM designs utilize two or more phases of processing logic to handle the current LPDDR4 data transfer rates, as one example using one phase of processing logic to capture data on the rising edge of the data transfer strobe, and another phase of processing logic to capture data on the falling edge of the strobe. One hidden limitation of such multi-phased processing embodiments is the difficulty of extracting difference-based information from consecutively received unit intervals, as consecutive unit intervals by definition are known only by different processing phases. Thus, multi-phased processing is problematic for both codes using transition-encoding, as well as embedded- or self-clocking data solutions that rely on comparison of data values received in consecutive unit intervals.

These issues of clock extraction, and transition- or change-detection are most intractable in the communications receiver embodiment, thus the examples herein focus on embodiments in which the relatively slow DRAM device is the receiver. No limitation is implied, as one familiar with the art will readily acknowledge that bidirectional data communication with DRAM devices is well understood, and that any example embodiment suitable for DRAM receive implementation could easily implement the simpler transmit requirements as well.

Receivers using Multi-input comparators

As described in [Holden I], a multi-input comparator with coefficients $a_0, a_1, \ldots, a_{m-1}$ is a circuit that accepts as its input a vector $(x_0, x_1, \ldots, x_{m-1})$ and outputs

$$\text{Result}=(a_0*x_0+\ldots+a_{m-1}*x_{m-1}) \quad \text{(Eqn. 1)}$$

In many embodiments, the desired output is a binary value, thus the value Result is sliced with an analog comparator to produce a binary decision output. Because this is a common use, the colloquial name of this circuit incorporates the term "comparator", although other embodiments may use a PAM-3 or PAM-4 slicer to obtain ternary or quaternary outputs, or indeed may retain the analog output of Eqn. 1 for further computation. In at least one embodiment, the coefficients are selected according to sub-channel vectors corresponding to rows of a non-simple orthogonal or unitary matrix used to generate the ODVS code.

As one example, [Ulrich I] teaches that the ODVS code herein called ENRZ may be detected using three instances of the same four input multi-input comparator, performing the operations

$$R_0=(A+C)-(B+D) \quad \text{(Eqn. 2)}$$

$$R_1=(C+D)-(A+B) \quad \text{(Eqn. 3)}$$

$$R_2=(C+B)-(D+A) \quad \text{(Eqn. 4)}$$

which may be readily performed with three identical instances of a multi-input comparator with coefficients of [+1 +1 −1 −1] and distinct permutations of the four input values as described in Eqn. 2-4.

ODVS Sub-Channels

It is conventional to consider the data input to encoder **112** of FIG. **1** as vectors of data (i.e., a data word) to be atomically encoded as a codeword to be transmitted across channel **120**, detected by receiver **132**, and ultimately decoded **138** to produce a received reconstruction of the transmitted vector or data word.

However, it is equally accurate to model the communications system in a somewhat different way. As this alternate model is most easily understood in a system not requiring a separate decoder, a particular embodiment based on the ENRZ code as illustrated in FIG. **2** will be used for purposes of description, with no limitation being implied. Elements in FIG. **2** functionally identical to elements of FIG. **1** are identically numbered, although FIG. **2** may subsequently illustrate additional internal structure or composition of features that are generically described in FIG. **1**

In FIG. **2**, input data vector **100** entering communications transmitter **110** is explicitly shown to be expanded to its individual bits S_0, S_1, S_2 and entering encoder **112**. Individual signals representing the symbols of the codeword output by encoder **112** are shown controlling individual line drivers **118** to emit signals onto wires **125** comprising communications channel **120**. As any one wire transporting the ENRZ code can take on one of four different signal values, two control signals are shown controlling each wire's line driver.

As previously noted, in this embodiment communications receiver **130** does not require an explicit decoder. The internal structure of receiver **132** is illustrated, comprising four receive front ends (as **131**) that accept signals from wires **125**, and optionally may include amplification and equalization, as required by the characteristics of the communications channel **120**. Three multi-input comparators are shown with their inputs connected to the four received wire signals as described by Eqns. 2, 3, and 4. For avoidance of confusion, the multi-input comparators are illustrated as including a computational function **133** followed by a slicing function **134** producing digital outputs R_0, R_1, R_2 from the computational combination of the input values.

One familiar with the art may note that the ODVS encoder accepts one set of input data and outputs one codeword per transmit unit interval. If, as is the case in many embodiments, the encoder includes combinatorial digital logic (i.e. without additional internal state,) this periodic codeword output may easily be seen as performing a sampling function on the input data followed by the encoding transformation, subsequent transmission, etc. Similarly, if the detection

operation within the receiver is similarly combinatorial, as is the case here with multi-input comparators performing the detection, the state of a given output element is solely determined by the received signal levels on some number of channel wires. Thus, each independent signal input (as one example, S_0) and its equivalent independent signal output (as R_0) may be considered a virtual communications channel, herein called a "sub-channel" of the ODVS encoded system. A given sub-channel may be binary (i.e. communicate a two-state value) or may represent a higher-ordered value. Indeed, as taught by [Shokrollahi IV], the sub-channels of a given ODVS code are sufficiently independent that they may utilize different alphabets (and sizes of alphabets) to describe the values they communicate.

All data communications in an ODVS system, including the state changes in sub-channels, are communicated as codewords over the entire channel. An embodiment may associate particular mappings of input values to codewords and correlate those mappings with particular detector results, as taught by [Holden I] and [Ulrich I], but those correlations should not be confused with partitions, subdivisions, or sub-channels of the communications medium itself.

The concept of ODVS sub-channels is not limited by the example embodiment to a particular ODVS code, transmitter embodiment, or receiver embodiment. Encoders and/or decoders maintaining internal state may also be components of embodiments. Sub-channels may be represented by individual signals, or by states communicated by multiple signals.

Timing Information on a Sub-Channel

As an ODVS communications system must communicate each combination of data inputs as encoded transmissions, and the rate of such encoded transmissions is of necessity constrained by the capacity of the communications medium, the rate of change of the data to be transmitted must be within the Nyquist limit, where the rate of transmission of codewords represents the sampling interval. As one example, a binary clock or strobe signal may be transmitted on an ODVS sub-channel, if it has no more than one clock edge per codeword transmission.

An embodiment of an ODVS encoder and its associated line drivers may operate asynchronously, responding to any changes in data inputs. Other embodiments utilize internal timing clocks to, as one example, combine multiple phases of data processing to produce a single high-speed output stream. In such embodiments, output of all elements of a codeword is inherently simultaneous, thus a strobe or clock signal being transported on a sub-channel of the code will be seen at the receiver as a data-aligned clock (e.g. with its transition edges occurring simultaneous to data edges on other sub-channels of the same code.) Similar timing relationships are often presumed in clock-less or asynchronous embodiments as well.

FIG. **3** is a block diagram of an ODVS communications system, in which a data-aligned strobe signal (comparable to the strobe associated with known LPDDR4 channels) is carried by a sub-channel, and N bits of data are carried on other sub-channels of the same code. At the receiver, a collection of multi-input comparators **132** detects the received information, outputting data **345** and a received data-aligned strobe **346**. Introduction of a one-half unit interval time delay **350** offsets the received strobe to produce an eye-aligned strobe **356** having a transition edge at the optimum sampling time to latch data **345**. As is conventional in many DRAM embodiments, two processing phases are shown for data sampling; phase **360** sampling data **345** on the negative edge of eye-aligned strobe **356**, and phase **370** sampling data **345** on the positive edge of eye-aligned strobe **356**. Methods of embodiment for delay **350** as well as any associated adjustment or calibration means it may require is well known in the art for LPDDR interfaces.

Mapping LPDDR Communications to an ODVS System

The existing LPDDR4 specification provides for eight data wires, one wire for DMI, and two Strobe wires, for a total of 11 wires. These legacy connections may be mapped to a new protocol mode, herein called LPDDR5, using ODVS encoding in several ways.

As taught by [Holden I], the noise characteristics of a multi-input comparator are dependent on its input size and configuration. [Shokrollahi IV] also teaches that the signal amplitudes resulting from various computations as Eqn. 1 can present different receive eye characteristics. Thus, preferred embodiments will designate a higher quality (e.g. wider eye opening) sub-channel to carry clock, strobe, or other timing information, when the characteristics of the available sub-channels vary.

Glasswing

A first embodiment, herein identified as Glasswing and shown in the block diagram of FIG. **4**, adds a new wire to provide a total of 12 wires that are then logically divided into two groups of six wires each. Each group of six wires is used to carry an instance of an ODVS code transmitting 5 bits on 6 wires (called the 5b6w code henceforth), thus providing a total of ten sub-channels. Eight sub-channels are used to carry eight bits of data, one sub-channel is used to carry a mask bit (conventionally used during DRAM write operations to block individual byte writes), and one sub-channel is used to carry a data-aligned strobe. The 5b6w code is balanced, all symbols within any given codeword summing to zero, and is structured such that each codeword contains exactly one +1 and one −1, the remaining codeword symbols being including +1/3 and −1/3 symbols. As will be apparent to one familiar with the art, multiple permutations of a suitable codeword set and corresponding comparator detection coefficients may be used in embodiments.

Each 5b6w receiver in Glasswing incorporates five multi-input comparators. In a preferred embodiment, the codewords of each instance of the 5b6w code are shown in Table 1 and the set of comparators are:

x0−x1
(x0+x1)/2−x2
x4−x5
x3−(x4+x5)/2
(x0+x1+x2)/3−(x3+x4+x5)/3

where the wires of each six wire group are designated as x0, x1 . . . x5.

TABLE 1

±[1, 1/3, −1/3, −1, −1/3, 1/3]	±[1, 1/3, −1/3, 1/3, −1, −1/3]
±[1/3, 1, −1/3, −1, −1/3, 1/3]	±[1/3, 1, −1/3, 1/3, −1, −1/3]
±[1/3, −1/3, 1, −1, −1/3, 1/3]	±[1/3, −1/3, 1, 1/3, −1, −1/3]
±[−1/3, 1/3, 1, −1, −1/3, 1/3]	±[−1/3, 1/3, 1, 1/3, −1, −1/3]
±[1, 1/3, −1/3, −1, 1/3, −1/3]	±[1, 1/3, −1/3, 1/3, −1/3, −1]
±[1/3, 1, −1/3, −1, 1/3, −1/3]	±[1/3, 1, −1/3, 1/3, −1/3, −1]
±[1/3, −1/3, 1, −1, 1/3, −1/3]	±[1/3, −1/3, 1, 1/3, −1/3, −1]
±[−1/3, 1/3, 1, −1, 1/3, −1/3]	±[−1/3, 1/3, 1, 1/3, −1/3, −1]

Additional information about this 5b6w code is provided in [Ulrich II].

8b9w

A second embodiment, herein identified as "8b9w" and shown in the block diagram of FIG. **5**, retains the existing LPDDR4 compliment of 11 data transfer wires. Nine wires

are used to carry an 8b9w code internally including a 5 wire code herein called the 4.5b5w code and a 4 wire code herein called the 3.5b4w code, which combined provides 288 distinct codeword combinations of which 257 will be used by the encoder. 256 of the codewords are used to encode 8 bits of data when the Mask input is false, and one codeword is used to mark a "do not write" condition when the Mask input is true. A data-aligned strobe is communicated using legacy means, using the two existing LPDDR4 strobe wires.

In at least one embodiment, each 4.5b5w receiver incorporates seven multi-input comparators, using the codewords of the 4.5b5w code as given in Table 2 and the set of comparators

x0−x1
x0−x2
x0−x3
x1−x2
x1−x3
x2−x3
(x0+x1+x2+x3)/4−x4

where the wires of each five wire group are designated as x0, x1 . . . x4.

TABLE 2

±[0, −1, 1, 1, −1]	±[−1, 1, 0, 1, −1]
±[0, 1, −1, 1, −1]	±[1, −1, 0, 1, −1]
±[0, 1, 1, −1, −1]	±[1, 1, 0, −1, −1]
±[−1, 0, 1, 1, −1]	±[−1, 1, 1, 0, −1]
±[1, 0, −1, 1, −1]	±[1, −1, 1, 0, −1]
±[1, 0, 1, −1, −1]	±[1, 1, −1, 0, −1]

The ISI-ratio of the first 6 comparators (as defined in [Hormati I]) is 2, whereas the ISI-ratio of the last comparator is 1.

In the same embodiments, the codewords of the 3.5b4w code are given in Table 3.

TABLE 3

±[1, −1, 0, 0]	±[0, 1, −1, 0]
±[1, 0, −1, 0]	±[0, 1, 0, −1]
±[1, 0, 0, −1]	±[0, 0, 1, −1]

Each 3.5b4w receiver incorporates six multi-input comparators. If the wires of each four wire group are designated as x0, x1 . . . x3, the comparators are:

x0−x1
x0−x2
x0−x3
x1−x2
x1−x3
x2−x3

The ISI-ratio of all these comparators (as defined in [Hormati I]) is 2.

ENRZ

A third embodiment, herein identified as "ENRZ" and shown in the block diagram of FIG. **6**, adds a new wire to the existing LPDDR4 compliment to provide a total of 12 wires that are then logically divided into three groups of four wires each. Each group of four wires is used to carry an instance of ENRZ code, each instance thus having eight unique codewords. In at least one embodiment, one codeword from each instance is reserved as a repeat code, with the seven remaining codewords per instance being combined by the encoder to provide 7*7*7=343 unique combinations, more than sufficient to encode eight data bits and a mask condition, as in the previous example. In another embodiment, there is no designated repeat codeword. Instead, the transmitter may store the last transmitted codeword, and produce for the following UI a codeword that is different from the transmitted one, as taught in [Shokrollahi III]. The Data-aligned strobe is used to clock codeword emission at the transmitter, with the repeat code being emitted on each instance whenever the present codeword to be emitted is identical to the codeword emitted in the previous unit interval. At the receiver, a known art clock recover circuit extracts timing information from received codeword edges, and a one data value history buffer regenerates duplicated data values for each instance on detection of a received repeat codeword.

Further description of this embodiment may be found in [Shokrollahi III].

FIGS. **7**A, **7**B, and **7**C provide a comparison of the various embodiments; with receive eye diagrams shown for Glasswing, ENRZ, and 8b9w embodiments, respectively, at signaling rates of 6.4 GBaud and 8.4 GBaud.

The examples presented herein illustrate the use of vector signaling codes for point-to-point wire communications. However, this should not been seen in any way as limiting the scope of the described embodiments. The methods disclosed in this application are equally applicable to other communication media including optical and wireless communications. Thus, descriptive terms such as "voltage" or "signal level" should be considered to include equivalents in other measurement systems, such as "optical intensity", "RF modulation", etc. As used herein, the term "physical signal" includes any suitable behavior and/or attribute of a physical phenomenon capable of conveying information. Physical signals may be tangible and non-transitory.

Embodiments

In at least one embodiment, a method **800** comprises receiving, at step **802**, a set of symbols of a codeword of a vector signaling code at a plurality of multi-input comparators (MICs), the set of symbols representing a transformation of an input vector with a non-simple orthogonal or unitary matrix, the input vector comprising a plurality of sub-channels, wherein at least one sub-channel corresponds to an input data signal and wherein at least one sub-channel corresponds to a data-aligned strobe signal, forming, at step **802** a set of MIC output signals based on a plurality of comparisons between a plurality of subsets of symbols of the codeword, wherein for each comparison, each subset of symbols has a set of input coefficients applied to it determined by a corresponding MIC, and wherein the set of MIC output signals comprises at least one data output signal and at least one received data-aligned strobe signal, and sampling, at step **806**, the at least one data output signal according to the at least one received data-aligned strobe signal.

In at least one embodiment, at least one data output signal is sampled on a rising edge of at least one received data-aligned strobe signal. In another embodiment, at least one output data signal is sampled on a falling edge of at least one received data-aligned strobe signal.

In at least one embodiment, the input vector comprises 4 sub-channels corresponding to input data signals and 1 sub-channel corresponding to a data-aligned strobe signal. In at least one embodiment, each symbol of the set of symbols has a value selected from a set of at least two values. In a further embodiment, each symbol of the set of symbols has a value selected from the set of values {+1, +1/3, −1/3, −1}.

In at least one embodiment, the sets of input coefficients for each MIC are determined by the non-simple orthogonal or unitary matrix.

In at least one embodiment, the codeword is balanced.

In at least one embodiment, the method further comprises forming a set of output bits by slicing the set of MIC output signals.

In at least one embodiment, the method further comprises receiving the input vector on a plurality of wires, generating, using an encoder, the set of symbols of the codeword representing a weighted sum of sub-channel vectors, the sub-channel vectors corresponding to rows of the non-simple orthogonal or unitary matrix, wherein a weighting of each sub-channel vector is determined by a corresponding input vector sub-channel, and providing the symbols of the codeword on a multi-wire bus.

In at least one embodiment, an apparatus comprises a multi-wire bus configured to receive a set of symbols of a codeword of a vector signaling code, the set of symbols representing a transformation of an input vector with a non-simple orthogonal or unitary matrix, the input vector comprising a plurality of sub-channels, wherein at least one sub-channel corresponds to an input data signal and wherein at least one sub-channel corresponds to a data-aligned strobe signal, a plurality of multi-input comparators (MICs) configured to form a set of MIC output signals based on a plurality of comparisons between a plurality of subsets of symbols of the codeword, wherein for each comparison, each subset of symbols has a set of input coefficients applied to the subset determined by a corresponding MIC, and wherein the set of MIC output signals comprises at least one data output signal and at least one received data-aligned strobe signal, and a plurality of sampling circuits configured to sample the at least one data output signal according to the at least one received data-aligned strobe signal.

In at least one embodiment, at least one sampling circuit is configured to sample at least one data output signal on a rising edge of at least one received data-aligned strobe signal. In another embodiment, at least one sampling circuit is configured to sample at least one output data signal on a falling edge of at least one received data-aligned strobe signal.

In at least one embodiment, the input vector comprises 4 sub-channels corresponding to input data signals and 1 sub-channel corresponding to a data-aligned strobe signal. In at least one embodiment, each symbol of the set of symbols has a value selected from a set of at least two values. In a further embodiment, each symbol of the set of symbols has a value selected from the set of values $\{+1, +1/3, -1/3, -1\}$.

In at least one embodiment, the sets of input coefficients of each MIC are determined by the non-simple orthogonal or unitary matrix.

In at least one embodiment, the codeword is balanced.

In at least one embodiment, the apparatus further comprises a plurality of slicers configured to generate a set of output bits by slicing the set of MIC output signals.

In at least one embodiment, an apparatus comprises a plurality of wires configured to receive an input vector, the input vector comprising a plurality of sub-channels, wherein at least one sub-channel corresponds to a data signal, and wherein at least one sub-channel corresponds to a data-aligned strobe signal, an encoder configured to generate a set of symbols of a codeword representing a weighted sum of sub-channel vectors, the sub-channel vectors corresponding to rows of a non-simple orthogonal or unitary matrix, wherein a weighting of each sub-channel vector is determined by a corresponding input vector sub-channel, and a plurality of line drivers configured to transmit the symbols of the codeword on a multi-wire bus.

We claim:

1. A method comprising:

receiving, at a plurality of multi-input comparators (MICs) via a multi-wire bus, a set of symbols of a codeword of a vector signaling code, the set of symbols representing a transformation of an input vector with a non-simple orthogonal or unitary matrix, the input vector comprising a plurality of sub-channels, wherein at least one sub-channel corresponds to an input data signal and wherein at least one sub-channel corresponds to a data-aligned strobe signal;

forming a plurality of MIC output signals, each data MIC output signal of the plurality of data MIC output signals generated by a corresponding MIC comparing a subset of symbols of the codeword, and wherein each data MIC has a set of respective data input coefficients corresponding to a respective subchannel;

generating a timing MIC output signal using a corresponding timing MIC connected to all the wires of the multi-wire bus to form a comparison of the set of symbols of the codeword, wherein the timing MIC has a set of timing input coefficients orthogonal to each set of respective data input coefficients to remove the at least one data signal from the timing MIC output signal; and

sampling the plurality of data MIC output signals according to the timing MIC output signal.

2. The method of claim **1**, wherein at least one data MIC output signal is sampled on a rising edge of the timing MIC output signal.

3. The method of claim **1**, wherein at least one data MIC output signal is sampled on a falling edge of the timing MIC output signal.

4. The method of claim **1**, wherein the input vector comprises 4 sub-channels corresponding to input data signals and 1 sub-channel corresponding to a data-aligned strobe signal.

5. The method of claim **1**, wherein each symbol of the set of symbols has a value selected from a set of at least two values.

6. The method of claim **5**, wherein each symbol of the set of symbols has a value selected from the set of values $\{+1, +1/3, -1/3, -1\}$.

7. The method of claim **1**, wherein the sets of respective data input coefficients and the set of timing input coefficients are determined by the non-simple orthogonal or unitary matrix.

8. The method of claim **1**, wherein the codeword is balanced.

9. The method of claim **1**, further comprising forming a plurality of output bits by slicing the plurality of data MIC output signals.

10. The method of claim **1**, further comprising:

receiving the input vector on a plurality of wires;

generating, using an encoder, the set of symbols of the codeword representing a weighted sum of sub-channel vectors, the sub-channel vectors corresponding to rows of the non-simple orthogonal or unitary matrix, wherein a weighting of each sub-channel vector is determined by a corresponding input vector sub-channel; and,

providing the symbols of the codeword on a multi-wire bus.

11. An apparatus comprising:

a multi-wire bus configured to receive a set of symbols of a codeword of a vector signaling code, the set of symbols representing a transformation of an input vector with a non-simple orthogonal or unitary matrix, the input vector comprising a plurality of sub-channels, wherein at least one sub-channel corresponds to an input data signal and wherein at least one sub-channel corresponds to a data-aligned strobe signal;

a plurality of data multi-input comparators (MICs) configured to form a plurality of data MIC output signals, each data MIC configured to compare a subset of symbols of the codeword, wherein each data MIC has a set of respective input coefficients corresponding to a respective subchannel;

a timing MIC connected to all the wires of the multi-wire bus, the timing MIC configured to generate a timing MIC output signal by comparing the set of symbols of the codeword, wherein the timing MIC has a set of timing input coefficients orthogonal to each set of respective data input coefficients to remove the at least one data signal from the timing MIC output signal; and

a plurality of sampling circuits configured to sample the plurality of data MIC output signals according to the timing MIC output signal.

12. The apparatus of claim 11, wherein at least one sampling circuit is configured to sample at least one data MIC output signal on a rising edge of the timing MIC output signal.

13. The apparatus of claim 11, wherein at least one sampling circuit is configured to sample at least one data MIC output signal on a falling edge of the timing MIC output signal.

14. The apparatus of claim 11, wherein the input vector comprises 4 sub-channels corresponding to input data signals and 1 sub-channel corresponding to a data-aligned strobe signal.

15. The apparatus of claim 11, wherein each symbol of the set of symbols has a value selected from a set of at least two values.

16. The apparatus of claim 15, wherein each symbol of the set of symbols has a value selected from the set of values $\{+1, +1/3, -1/3, -1\}$.

17. The apparatus of claim 11, wherein the sets of respective data input coefficients and the set of timing input coefficients are determined by the non-simple orthogonal or unitary matrix.

18. The apparatus of claim 11, wherein the codeword is balanced.

19. The apparatus of claim 11, further comprising a plurality of slicers configured to generate a set of output bits by slicing the set of data MIC output signals.

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